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10/670,495	09/24/2003	Nir N. Shavit	6000-31700	7998

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,495	SHAVIT ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-106* is/are pending in the application.

4a) Of the above claim(s) *34-51 and 67-106* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,14-22,24,26,29-33,52-55,57 and 60-66* is/are rejected.

7)☒ Claim(s) *10,12,13,25,27,28,56,58 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-22 and 24-106 are pending in the Application.

Of the pending claims, claims 34-51, and 67-106 are withdrawn in response to Examiner's restriction requirement.

Claims 23 and 107-110 are cancelled.

Claims 1-4, 7, 10, 12, 15, 19, 20-22, 24-33, 52, 53, 55, 60, 63 and 66 are amended.

Claims 1-9, 11, 14-22, 24, 26, 29-33, 52-55, 57 and 60-66 are rejected.

Claims 10, 12, 13, 25, 27, 28, 56, 58 and 59 are objected to.

Response to Amendment

2. Applicant's amendments and arguments filed on 6 December 2006 in response to the office action mailed on 6 September 2006 (with respect to the section 102(b) rejections) have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments. Applicant's amendments and arguments with respect to the section 103(a) rejections have been fully considered, but are moot in view of the new ground(s) of rejection. Applicant's amendments and arguments with respect to the section 101 rejections, 112 second paragraph rejections, and claim objections are persuasive, therefore these objections and rejections have been withdrawn.

Specification

3. The previous objections to the specification (i.e. abstract and specification failing to provide proper antecedent basis for the claimed subject matter) are hereby removed in view of the amendments and arguments set forth by Applicant.

Claim Objections

4. Claims 1-20, 24-30 and 52-66 are objected to because of the following informalities:

As for claim 1, the phrase "application values" as recited in line 16 should be changed to "application value" for clarity. A similar rejection applies to claim 52.

As for claim 9, the phrase "the linearization point" as recited in lines 2-3 should be changed to "a linearization point" to properly establish antecedent basis for the phrase.

As for claims 24, and 27-30, the dependency of these claims should be changed to from "claim 23" to "claim 21" as claim 23 is no longer pending in the Application.

The remaining dependant claims are objected to for further limiting a previously objected to claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 21 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by MacGregor et al. (US Patent 4,584,640), hereinafter MacGregor.

As for claim 21, MacGregor teaches a system comprising:

a processor (Fig. 1, element 12); and

memory coupled to the processor, wherein the memory comprises program instructions executable by the processor to implement (processor is depicted in Fig. 2, the buffer and ROMs (elements 38, 36 and 34) store the instructions);

a k-compare, single-swap synchronization, wherein to implement the k-compare, single-swap synchronization the program instructions are configured to perform at least one and no more than two (2) atomic, single-location read-modify-write synchronizations (referring to Fig. 3A and 3B, Macgregor teaches performing a compare and swap operations via two single-location RWM cycles – col. 6, lines 16-52);

an update mechanism configured to update a state of a first targeted location (Figs. 3A and 3B – values are updated upon their storage in the registers. Additionally, compare and swap operations are performed on two locations hence a first and second location are analyzed and updated during the compare and swap operations – col. 2, lines 16-42 and abstract); and

a snapshot mechanism configured to verify a state of k-1 other targeted locations, wherein k is greater than 1 (assuming k=2, MacGregor teaches verifying the state of the other location as his invention is directed to compare and swap of **two** locations – see col. 2, lines 17-42 and abstract).

As for claim 31, MacGregor teaches the single-location synchronizations are compare-and-swap (CAS) synchronizations (col. 2, lines 16-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 9, 11, 14-17, 24, 26, 29, 30, 52, 53, 55, 57, 60-63, 66, are rejected under 35 U.S.C. 103(a) as being unpatentable over Afek et al. ("Atomic Snapshots of Shared Memory," Journal of the ACM, vol. 40, no. 4, pp. 873-890,1993), hereinafter Afek, and in further view of MacGregor (US Patent 4,584,640).

As for claims 1 and 52, Afek teaches a method (and computer program product) for providing a linearizable multi-compare, single-swap facility for concurrent software, the method comprising:

snapshotting a plurality of application values corresponding to a respective plurality of targeted memory locations to determine whether any of the application values are changed between two successive reads at the

targeted memory locations (page 878, "observation 1." Through page 879, "observation 2" – 2 sequential reads of the entire memory is performed to determine if any changes occur (this includes the data, update value "d", sequence number "k", and three register data structures "r_x"). If no change occurs the retuned values are considered to be a snapshot).

wherein said snapshotting comprises reading each of the plurality the application values at least twice and comparing each application values across pairs of successive reads (two successive collect operations must be performed before a snapshot will occur - page 878, "observation 1." Through page 879, "observation 2");

Afek additionally teaches updating a first application value corresponding to a first targeted memory location only if said snapshotting indicates that the plurality of application values remain unchanged between two successive reads at the targeted locations, wherein the first targeted memory location is distinct from the plurality of targeted locations (if two consecutive collects (i.e. reads) indicate no change (i.e. returning the same value) the r-toggle bit is changed) – Pages 882 and 884 (All sections under the heading "the bounded single-writer algorithm).

Lastly though Afek teaches ensuring that the first application value remains unchanged across said snapshotting (page 878, "observation 1." Through page 879, "observation 2"- two successive collect operations must be performed before a snapshot will occur), he fails to specifically teach the use of a pair of single-location synchronizations as recited by Applicant.

MacGregor however teaches a method and apparatus for a compare and swap instruction which includes utilizing single-location synchronizations (referring to Figs. 3A and 3B – values are updated upon their storage in the registers. Additionally, compare and swap operations are performed on two locations hence a first and second location are analyzed and updated during the compare and swap operations – col. 2, lines 16-42 and abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Afek to further include MacGregor's compare and swap method into his own system for atomic snapshots of shared memory. By doing so Afek could exploit the benefits increasing the speed of traversing data stored within specific data structures (such as a doubly-linked list) as taught by MacGregor in col. 1, lines 29-41.

As for claims 2, 15, 30 and 61, MacGregor teaches wherein the first targeted location and at least one of the other targeted locations are non-contiguous (col. 5, lines 8-14).

As for claim 3, MacGregor teaches wherein a first one of the single target synchronizations precedes the snapshotting, and wherein a second one of the single target synchronizations follows the snapshotting (Fig. 3B - the RMW command write occurs before the write operation).

As for claim 4, MacGregor teaches wherein the second one of the single target synchronizations effectuates the updating (Fig. 3B, col. 6, lines 26-53)

As for claim 5, MacGregor teaches wherein the single-location synchronizations retry on failure (Fig. 3A, system will retry upon bus failure).

As for claims 9, 24, and 55, MacGregor teaches displacing the first application value from the first targeted location prior to the linearization point of the snapshotting (Fig. 3B - the RMW command write occurs before the write operation).

As for claims 11, 26 and 57, MacGregor teaches wherein the displacing is performed by a load-linked sequence that employs one of the single-location synchronizations (col. 6, lines 26-52).

As for claims 14, 29 and 60, MacGregor teaches wherein any particular application value is read either from a corresponding one of the targeted locations, if encoded therein, or from an auxiliary location associated with an id, if instead, the id is encoded therein (col. 6, lines 26-52).

As for claim 16 and 63, MacGregor, teaches the single-location synchronizations are compare-and-swap (CAS) synchronizations (col. 2, lines 16-42).

As for claims 17 and 62, MacGregor the single-location synchronizations as being atomic read-modify-write synchronizations (col. 6, lines 25-35).

As for claim 53, MacGregor teaches his system as employing no more than two (2) atomic, single-location read-modify-write synchronizations (referring to Fig. 3A and 3B, Macgregor teaches performing a compare and swap operations via two single-location RWM cycles).

As for claim 66, MacGregor teaches the medium as including a disk (Fig. 1, element 26).

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Afek to further include MacGregor's compare and swap method into his

own system for atomic snapshots of shared memory. By doing so Afek could exploit the benefits increasing the speed of traversing data stored within specific data structures (such as a doubly-linked list) as taught by MacGregor in col. 1, lines 29-41.

7. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) as applied to claim 21 above, and in further view of Yeh et al. (US PG Publication 2003/0105943 A1), hereinafter Yeh.

As for claims 32-33, though MacGregor teaches all the limitations of the base claim, he fails to teach wherein the single-location synchronizations are compare-and-swap (CAS) synchronizations employed to define a load-linked (LL) sequence and a store-conditional (SC) sequence, respectively. Yeh however teaches a mechanism for processing speculative LL and SC instructions in a pipelined processor employing both LL and SC operations (paragraphs 0010 through 0011, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Yeh's mechanism for processing speculative LL and SC instructions into his own compare and swap system. By doing so, MacGregor would benefit by having a more effective means of monitoring system addresses, while avoiding the possibility of ceasing the monitoring operation should an exception occurs as taught by Yeh in paragraph 0009, all lines.

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) as applied to claim 21 above, and in further view of Bonola (Us.PG Publication 2003/0065892 A1)

As for claim 22, though MacGregor teaches all the limitations of claim 21, he fails to teach employing tagged id displacement for ABA avoidance. Bonola however teaches the use of tagged ids for ABA avoidance (paragraph 0013, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Bonola's Non-blocking FIFO array into his own system for compare and swap operations. By doing so, MacGregor would be able to further avoid deadlock situations as discussed by Bonola in paragraph 0010, all lines.

9. Claims 6-8, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching of Afek ("Atomic Snapshots of Shared Memory," Journal of the ACM, vol. 40, no. 4, pp. 873-890,1993) and MacGregor (US Patent 4,584,640) and as applied to claims 1 and 52 above, and in further view of Bonola (US PG Publication 2003/0065892 A1)

As for claims 6, and 7, though the combined teachings of Afek and MacGregor teach all the limitations of the base claims, they fail to teach employing a non-blocking property including obstruction-freedom. Bonola however teaches a concurrent non-blocking FIFO array which employs a non-blocking queue for obstruction freedom (paragraph 0026, all lines).

As for claims 8 and 54, though the combined teachings of Afek and MacGregor teach all the limitations of the base claims, they fail to teach the single-location synchronizations as employing tagged id displacement for ABA avoidance. Bonola however teaches the use of tagged ids for ABA avoidance (paragraph 0013, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Afek and MacGregor to further include Bonola's Non-blocking FIFO array. By doing so, Afek in view of MacGregor would be able to further avoid deadlock situations as discussed by Bonola in paragraph 0010, all lines.

10. Claims 18,19, 64, 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Afek ("Atomic Snapshots of Shared Memory," Journal of the ACM, vol. 40, no. 4, pp. 873-890,1993) and MacGregor (US Patent 4,584,640) as applied to claims 1 and 52 above, and in further view of Yeh (US PG Publication 2003/0105943 A1).

As for claims 18,19, 64 and 65 though the combined teachings of Afek and MacGregor teach all the limitations of the base claims, they fail to teach wherein the single-location synchronizations are compare-and-swap (CAS) synchronizations employed to define a load-linked (LL) sequence and a store-conditional (SC) sequence, respectively. Yeh however teaches a mechanism for processing speculative LL and SC instructions in a pipelined processor employing both LL and SC operations (paragraphs 0010 through 0011, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teachings of Afek and MacGregor to further include Yeh's mechanism for processing speculative LL and SC instructions. By doing so, Afek in view of MacGregor would benefit by having a more effective means of monitoring system addresses, while avoiding the possibility of ceasing the monitoring operation should an exception occurs as taught by Yeh in paragraph 0009, all lines.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Afek ("Atomic Snapshots of Shared Memory," Journal of the ACM, vol. 40, no. 4, pp. 873-890,1993), MacGregor (US Patent 4,584,640) and Yeh (US PG Publication 2003/0105943 A1) as applied to claim 19, and in further view of and in further view of Bonola (US PG Publication 2003/0065892 A1).

As for claim 20 though the combined teachings of Afek, MacGregor and Yeh teach all the limitations of the base claims, to teach employing tagged id displacement for ABA avoidance. Bonola however teaches the use of tagged ids for ABA avoidance (paragraph 0013, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for the combined teaches of Afek, MacGregor and Yeh to further include Bonola's Non-blocking FIFO array into his own system for compare and swap operations. By doing so, MacGregor would be able to further avoid deadlock situations as discussed by Bonola in paragraph 0010, all lines.

Response to Arguments

12. Applicant's amendments and arguments with respect to the Section 102(b) rejections have been fully considered, but they are not persuasive.

As for claims 21 and 52, Applicant asserts "MacGregor fails to teach anything regarding a snapshot mechanism configured to verify a state of k-1 other targeted locations, where k is greater than 1. Instead, MacGregor teaches verifying only to two locations two be swapped. In contrast Applicants claim

recites verifying the state of a plurality of locations other than the first targeted location to be updated."

This argument however is not persuasive. Assuming k=2, MacGregor teaches verifying the state of the other location, as his invention is directed to compare and swap of **two** locations – see col. 2, lines 17-42 and abstract. The rejection is therefore maintained based on the rationale supported by the arguments and rejection set forth *supra*.

13. Applicant's amendments and arguments with respect to the Section 103(a) rejections have been fully considered moot in view of the new ground(s) of rejection.

Allowable Subject Matter

14. Claims 10, 12, 13, 25, 27, 28, 56, 58 and 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
2-27-07

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW